CLAIMS

What is claimed is:

1. An integrated circuit tester apparatus comprising

a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random;

a second memory for storing therein deterministic test vector data;

a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number; and

a selector circuit for generating a test vector for application to an integrated circuit, said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output for coupling to said integrated circuit.

2. An integrated circuit tester apparatus as described in Claim 1 wherein said selector circuit is a multiplexer and wherein said multiplexer has a first data input coupled to said random number generator, a second data input coupled to said second memory, and a selector input coupled to said first memory, said multiplexer for passing through to said output a bit value of said first data input provided said selector input receives a first bit value and for passing through to

said output a bit value of said second data input provided said selector input receives a second bit value.

3. An integrated circuit tester apparatus as described in Claim 1 wherein said random number generator is a linear feedback shift register (LFSR).

4. An integrated circuit tester apparatus as described in Claim 1 wherein said mask vector is data compressed.

5. An integrated circuit test apparatus as described in Claim 4 and further comprising a decompressor coupled between said first memory and said selector circuit.

6. An integrated circuit tester apparatus as described in Claim 1 wherein said deterministic test vector data is generated by an automatic test pattern generator (ATPG) process and downloaded into said second memory.

7. In integrated circuit testing system comprising:

a) an integrated circuit tester comprising:

a1) a first memory for storing therein a mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random; and

a2) a second memory for storing therein deterministic test vector data, said first and second memory coupled to a port;

b) an integrated circuit device under test (DUT) comprising:

b1) a circuit block to be tested;

b2) a random number generator for generating a reproducible sequence of pseudo random bits based on a seed number; and

b3) a selector circuit coupled to said port and for generating a test vector for application to said circuit block, said selector circuit for selecting bits as between said random number generator and said second memory based on said mask vector, said selector circuit having an output coupled to said circuit block.

8. An integrated circuit testing system as described in Claim 7 wherein said selector circuit is a multiplexer and wherein said multiplexer has a first data input coupled to said random number generator, a second data input coupled to said second memory, and a selector input coupled to said first memory, said multiplexer for passing through to said output a bit value of said first data input provided said selector input receives a first bit value and for passing through to said output a bit value of said second data input provided said selector input receives a second bit value.

9. An integrated circuit testing system as described in Claim 7 wherein said random number generator is a linear feedback shift register (LFSR).

10. An integrated circuit testing system as described in Claim 7 wherein an output of said circuit block is coupled to an input of one stage of said LFSR.

11. An integrated circuit testing system as described in Claim 7 wherein said mask vector is data compressed.

12. An integrated circuit testing system as described in Claim 11 and further comprising a decompressor coupled between said first memory and said selector circuit.

13. An integrated circuit testing system as described in Claim 7 wherein said deterministic test vector data is generated by an automatic test pattern generator (ATPG) process and downloaded into said second memory.

14. A method for testing an integrated circuit comprising the steps of:

a) retrieving a mask vector from a first memory, said mask vector for characterizing corresponding test vector data, said mask vector comprising a plurality of bit positions wherein a first bit value indicates that said corresponding test vector data is deterministic and wherein a second bit value indicates that said corresponding test vector data is pseudo random;

b) retrieving deterministic test vector data from a second memory;

c) initializing a random number generator with a seed number and thereafter generating a reproducible sequence of pseudo random bits based on said seed number; and

d) generating an output test vector for application to a circuit block of said integrated circuit, said step d) comprising the step of selecting bits as between said random number generator and said second memory based on said mask vector.

15. A method as described in Claim 14 further comprising the steps of:

e) applying said output test vector to said circuit block;

f) obtaining an output generated by said circuit block in response to said output test vector;

g) verifying said circuit block by comparing said output generated by said circuit block to a reference output.

16. A method as described in Claim 14 wherein said random number generator is a linear feedback shift register (LFSR).

17. A method as described in Claim 14 further comprising the steps of:

applying said output test vector to said circuit block;

obtaining an output generated by said circuit block in response to said output test vector;

supplying said output generated by said circuit block to an input of a stage of said LFSR.

18. A method as described in Claim 14 wherein said mask vector is data compressed on said first memory and wherein said step a) comprises the steps of:

a1) reading said mask data from said first memory; and

a2) decompressing said mask vector data.

19. A method as described in Claim 14 wherein said deterministic test vector data is generated by an automatic test pattern generator (ATPG) process and downloaded into said second memory.

20. A method as described in Claim 14 wherein said steps c) and d) are performed within said integrated circuit.